Input clamps

The R, G, B respectively (R−Y), Y and (B−Y) video signals are AC-coupled to the IC where they are clamped on the black level. The timing information for this clamping action is derived from the associated synchronization signal SYNC, which could also consist of the composite video information signal CVBS. The syncsignal is AC-coupled to the IC where it is clamped on top-sync level, information obtained from this action is used to generate the clamp pulses.

The clamp pulses can be generated in two ways:

1. Using the sync information (internal clamping)

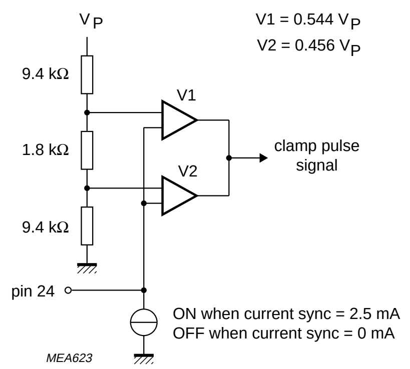
   The sync information is clamped on top-sync and the information obtained from this action is used to switch an internal current source at pin 24.

   Pin 24 should be connected to V_P via a 4.7 kΩ resistor, and a 1 nF capacitor to ground. During video scan the voltage at pin 24 will be HIGH (equals positive supply voltage). During the synchronization pulses the voltage at pin 24 will drop to zero because of the current sink (2.5 mA).

   When the synchronization pulse is over, the current source is switched off and the voltage at pin 24 will rise to its higher level. Because of the time constant at pin 24, the restoration will take some microseconds. The voltage at pin 24 is also sensed internally and at the time it is between $0.456V_P$ and $0.544V_P$, a time pulse is generated and used for the clamping action.

2. Using a sandcastle pulse (external clamping)

   If an associated sandcastle pulse is available, it can also be used as a clamping pulse. In this event the sandcastle pulse should be connected to pin 24, the top of the clamping pulse should be between $0.544V_P$ and $0.456V_P$. The timing of the internal clamping pulse will be equal to the timing of the higher part of the sandcastle pulse. If the sync signal is also connected, the current sink will also become active during the synchronization pulses. This means that the sandcastle pulse should be connected to pin 24 via a 1 kΩ dropping resistor. In this event only the sandcastle pulse at pin 24 will be influenced during sync pulses, but the sandcastle pulse at the sandcastle source will be unchanged.



Tolerance on V1 and V2 is given by ΔR/R and $\Delta V_P/V_P$. The diffusion process gives ΔR/R (max) = 1.5%.

Fig.7 Clamping circuit.

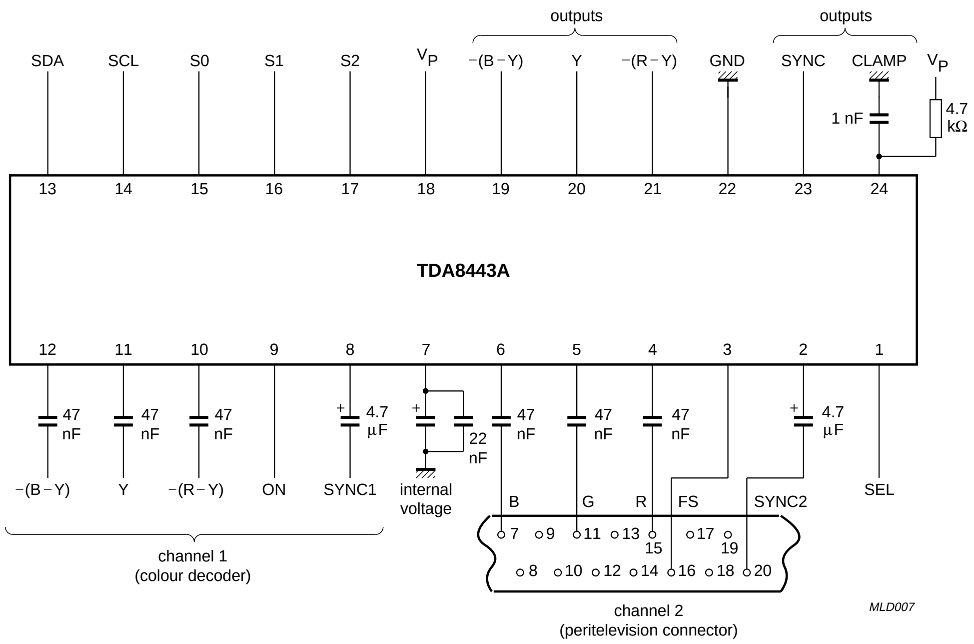


Fig.6 Application diagram (example).

APPLICATION INFORMATION

Table 10 Channel input/output information

INPUT 1	INPUT 2	OUTPUT	MODE	D5	D4	D3
Y = 0.34 V U = –1.33 V V = –1.05 V S = 0.3 V	–	Y = 0.34 V U = –1.33 V V = –1.05 V S = 0.6 V	2	1	1	1
–	R = 0.75 V G = 0.75 V B = 0.75 V S = 0.3 V	Y = 0.34 V U = –1.33 V V = –1.05 V S = 0.6 V	1	1	1	1
Y = 0.34 V U = –1.33 V V = –1.05 V S = 0.3 V	–	Y = 0.68 V U = –2.66 V V = –2.10 V S = 0.6 V	2	1	0	0
–	R = 0.75 V G = 0.75 V B = 0.75 V S = 0.3 V	Y = 0.68 V U = –2.66 V V = –2.10 V S = 0.6 V	1	1	0	0
Y = 0.34 V U = –1.33 V V = –1.05 V S = 0.3 V	–	Y = 0.34 V U = –1.33 V V = –1.05 V S = 0.6 V	2	1	0	1
–	Y = 0.34 V U = –1.33 V V = –1.05 V S = 0.3 V	Y = 0.34 V U = –1.33 V V = –1.05 V S = 0.6 V	0	1	0	1
Y = 0.34 V U = –1.33 V V = –1.05 V S = 0.3 V	–	Y = 0.68 V U = –2.66 V V = –2.10 V S = 0.6 V	2	1	1	0
–	Y = 0.34 V U = –1.33 V V = –1.05 V S = 0.3 V	Y = 0.68 V U = –2.66 V V = –2.10 V S = 0.6 V	0	1	1	0

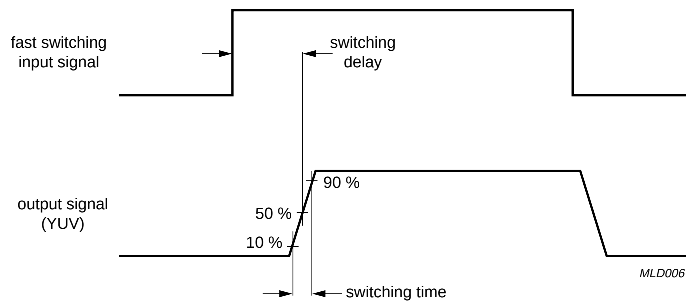


Fig.5 Fast switching signal diagram.

TIMING CHARACTERISTICS

I^2C-bus load conditions: 4 kΩ pull-up resistor to +5 V; 200 pF capacitor to GND;
all values are referenced to V_{IH} = 3 V and V_{IL} = 1.5 V; see Fig.4.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.
t_{BUF}	time bus must be free before start		4.7	–	µs
$t_{SU;STA}$	set-up time for start condition		4.7	–	µs
$t_{HD;STA}$	hold time for start condition		4.0	–	µs
t_{LOW}	SCL and SDA LOW time		4.7	–	µs
t_{HIGH}	SCL HIGH time		4.0	–	µs
t_r	SCL and SDA rise time		–	1.0	µs
t_f	SCL and SDA fall time		–	0.3	µs
$t_{SU;DAT}$	data set-up time (write)		250	–	ns
$t_{HD;DAT}$	data hold time (write)	note 1	1.0	–	µs
$t_{SU;ACK}$	acknowledge set-up time		–	2	µs
$t_{HD;ACK}$	acknowledge hold time		0	–	µs
$t_{SU;STO}$	set-up time for stop condition		4.7	–	µs

Note

1. Timing $t_{HD;DAT}$ deviates from the I^2C-bus specification. After reset has been activated, a delay of 50 µs must occur before transmission may be resumed.

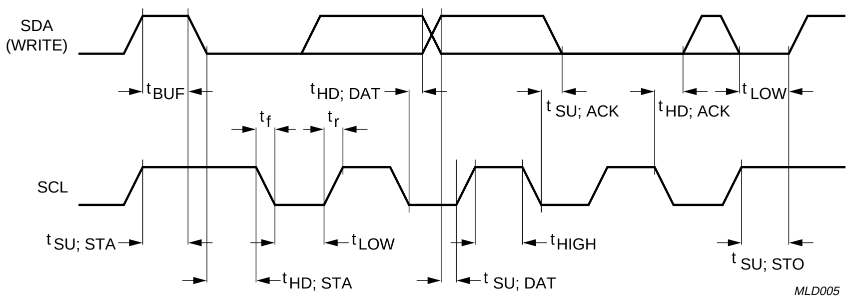


Fig.4 I^2C-bus timing diagram.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Select input						
V_{IH}	HIGH level input voltage		3	–	V_P	V
V_{IL}	LOW level input voltage		–0.3	–	0.4	V
I_{IH}	HIGH level input current		–	0	10	μA
I_{IL}	LOW level input current		–50	–10	0	μA
ON input						
V_{IH}	HIGH level input voltage		3	–	V_P	V
V_{IL}	LOW level input voltage		–0.3	–	1.5	V
I_{IH}	HIGH level input current		–	–	10	μA
I_{IL}	LOW level input current		–	–	10	μA

Notes

1. Crosstalk is defined as the unwanted data transfer from an output, driven at nominal level, to other inputs and outputs on the IC and is expressed as a ratio in dBs.
2. Signal-to-noise ratio = $20\log\frac{V_{o(p-p)}}{V_{no(rms)}}$ (B = 5 MHz)
3. Supply voltage ripple rejection = $20\log\frac{V_{RR(supply)}}{V_{RR(at\ the\ output)}}$

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$G_{diff(p-p)}$	differential gain at nominal output signals (peak-to-peak value)	R–Y = 1.05 V (p-p)	–	–	10	%
		B–Y = 1.33 V (p-p)	–	–	10	%
		Y = 0.34 V (p-p)	–	–	10	%
S/N	signal-to-noise ratio	nominal input; B = 5 MHz; note 2	50	–	–	dB
SVRR	supply voltage ripple rejection	note 3	30	–	–	dB
V_O	DC output levels during clamping		–	5.3	–	V
Synchronization channels						
G_{diff}	gain difference (programmed value)		–	–	10	%
B	bandwidth	–3 dB	–	50	–	MHz
		+3 dB; gain × 1	–	20	–	MHz
		±3 dB; gain × 2	–	13	–	MHz
$V_{i(p-p)}$	input amplitude of sync signal for correct operation of clamp pulse generator (peak-to-peak value)		0.2	–	2.5	V
$\|Z_{23-22}\|$	output impedance (pin 23)		–	20	30	Ω
$V_{o(p-p)}$	maximum undistorted output amplitude (pin 23) (peak-to-peak value)		2.5	–	–	V
V_O	DC output level on top of sync pulse		1.5	1.9	2.4	V
I²C-bus inputs for SDA, SCL						
V_{IH}	HIGH level input voltage		3	–	V_P	V
V_{IL}	LOW level input voltage		–0.3	–	1.5	V
I_{IH}	HIGH level input current		–	–	10	μA
I_{IL}	LOW level input current		–	–	10	μA
I²C-bus output for SDA (open collector)						
V_{OL}	LOW level output voltage	I_{OL} = 3 mA	–	–	0.4	V
Address selection inputs for S0, S1, S2						
V_{IH}	HIGH level input voltage		3	–	V_P	V
V_{IL}	LOW level input voltage		–0.3	–	0.4	V
I_{IH}	HIGH level input current		–	0	10	μA
I_{IL}	LOW level input current		–50	–10	0	μA
Fast switching input						
V_{IH}	HIGH level input voltage		1	–	3	V
V_{IL}	LOW level input voltage		–0.3	–	0.4	V
I_{IH}	HIGH level input current		–	0	500	μA
I_{IL}	LOW level input current		–100	–	–	μA
t_{sw}	switching time	see Fig.5	–	10	–	ns
t_d	switching delay	see Fig.5	–	20	–	ns

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_P	supply voltage (pin 18)	–	14	V
$V_{I(SDA)}$	input voltage (pin 13)	–0.3	14	V
$V_{I(SCL)}$	input voltage (pin 14)	–0.3	14	V
V_n	input voltage any other pin	–0.3	V_P + 0.3	V
$I_{O(max)}$	maximum output current	–	20	mA
T_{amb}	operating ambient temperature	0	+70	°C
T_{stg}	IC storage temperature range	–55	+125	°C
T_j	maximum junction temperature	–	+125	°C

CHARACTERISTICS

V_P = 12 V; T_{amb} = 25 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_P	supply voltage (pin 18)		10.8	12.0	13.2	V
I_P	supply current		–	65	90	mA
RGB/YUV channels						
G_{abs}	absolute gain difference (programmed value)		–	0	10	%
G_{rel}	relative gain difference	between Y output and the (R–Y) and (B–Y) channel outputs	–	0	10	%
		between any other two channels	–	0	5	%
I_I	input current		–	0.5	1.0	μA
$\|Z_{19-22}\|$	output impedance (pin 19)		–	7	30	Ω
$\|Z_{20-22}\|$	output impedance (pin 20)		–	7	30	Ω
$\|Z_{21-22}\|$	output impedance (pin 21)		–	7	30	Ω
B	bandwidth	–3 dB; mode 0 or 2	–	25	–	MHz
		+3 dB; mode 0 or 2	–	12	–	MHz
		±3 dB; mode 1	–	10	–	MHz
t_{diff}	mutual time difference at output	all inputs of one source connected together	–	–	25	ns
$V_{o(p-p)}$	maximum output amplitude of YUV signals (peak-to-peak value)	gain × 1	2.1	–	–	V
		gain × 2	4.2	–	–	V
α_{ct}	crosstalk	note 1; f_i = 5 MHz; between inputs of same source	–	–	–30	dB
		note 1; between same source	–	–	–40	dB
α_{off}	isolation (OFF state)	f_i = 10 MHz	50	–	–	dB

Table 5 Priority/fast switching bit D2

D2	FAST SWITCHING (PIN 3)	MODE
0	X(1)	0 to 2, depending on D7, D6
1	0.4 V	2

Note

1. X = don't care.

Table 6 Output state control bits

D1	D0	PIN 9	FUNCTION
0	X(1)	X(1)	OFF
1	0	L	OFF
1	0	H	ON
1	1	X(1)	ON

Note

1. X = don't care.

Power-on reset

If the circuit is switched on in the I²C-bus mode, all bits of D0 to D7 are set to zero.

Table 7 Non-I²C-bus mode (S2 = S1 = S0 = L)

CONTROL			MODE SWITCHED BY FS (PIN 3)	GAIN SETTINGS		B1, B3	B2
PIN 13	PIN 14	PIN 1		A1	A4, A3, A2		
L	L	L	2 or 0	1	1	1	1
L	L	H	2 or 0	1	2	1	1
L	H	L	2 or 1	1	1	–1	0.45
L	H	H	2 or 0	1	1	–1	0.45
H	L	L	2 or 0	2	1	1	1
H	L	H	2 or 0	2	2	1	1
H	H	L	2 or 1	2	1	–1	0.45
H	H	H	2 or 0	2	1	–1	0.45

Table 8 Fast switching input (pin 3)

FS	MODE SELECTED
≤0.4 V	mode 2
1 to 3 V	mode 0 or mode 1 as set by control

Table 9 ON input (pin 9)

ON	FUNCTION
L	OFF; no output signal; high impedance OFF-state
H	function is determined in Table 7

Table 2 Address selection

ADDRESS SELECT PINS[1][2]			ADDRESS SELECT BITS		
S2 (PIN 17)	**S1 (PIN 16)**	**S0 (PIN 15)**	**MA2**	**MA1**	**MA0**
L	L	L	∗[3]	∗[3]	∗[3]
L	L	H	0	0	1
L	H	L	0	1	0
L	H	H	0	1	1
H	L	L	1	0	0
H	L	H	1	0	1
H	H	L	1	1	0
H	H	H	1	1	1

Notes

1. L = LOW level input voltage.
2. H = HIGH level input voltage.
3. ∗ = non-I^2C-bus operation.

Table 3 Mode control bits D7 and D6

MODE	D7	D6	FUNCTION
0	0	0	Channel 2 selected, no matrix
1	0	1	Channel 2 selected, matrix active
2	1	0	Channel 1 selected
–	1	1	not allowed

Table 4 Gain setting (see also Table 9)

D5	D4	D3	A1	A2, A3, A4	B1, B3	B2
0	0	0	1	1	–1	0.45
0	0	1	1	1	1	1
0	1	0	not allowed		–	–
0	1	1	1	1	–1	0.45
1	0	0	2	2	–1	0.45
1	0	1	2	1	1	1
1	1	0	2	2	1	1
1	1	1	2	1	–1	0.45

Matrix equations

The relationship between output and input signals of the matrix is as follows:

$Y = 0.3R + 0.59G + 0.11B$

$R–Y = 0.7R – 0.59G – 0.11B$

$B–Y = –0.3R – 0.59G + 0.89B$

FUNCTIONAL DESCRIPTION

The circuit contains two sets of inputs (see Fig.1). Both channels can receive RGB or YUV signals. Each set of inputs has its own synchronization input, which internally generates a pulse to clamp the inputs. The internal clamping pulse can also be controlled by a signal (e.g. a sandcastle pulse) applied to pin 24. The pulse will occur during the time that the signal at pin 24 is between 5.5 and 6.5 V. If both a sync signal and a pin 24 signal are used the signal should be applied to pin 24 via a 1 kΩ resistor.

RGB signals of Channel 2 can be matrixed to YUV signals.

The outputs can be set in a high impedance OFF state, which allows the use of seven devices in parallel (I^2C-bus mode).

The circuit can be controlled by an I^2C-bus compatible microcontroller or directly by DC voltages. The fast switching input can be operated via pin 16 of the peritelevision connector.

I^2C-bus mode

The protocol for the devices in I^2C-bus mode is shown in Fig.3.

Table 1 Protocol bit description

BIT	DESCRIPTION
STA	start condition
MA2 to MA0	address selection bits; see Table 2
ACK	acknowledge bit
D7	channel selection bit; see Table 3
D6	matrix selection bit; see Table 3
D5 to D3	gain control bits; see Table 4
D2	fast switching priority bit; see Table 5
D1 and D0	output state control bits; see Table 6
STO	stop condition

STA	1	1	0	1	MA2	MA1	MA0	0	ACK	D7	D6	D5	D4	D3	D2	D1	D0	ACK	STO

MSA003

See Table 1.

Fig.3 I^2C-bus protocol.

PINNING

SYMBOL	PIN	DESCRIPTION
SEL	1	select input (non-I²C-bus mode only)
SYNC2	2	synchronization input for Channel 2
FS	3	fast switching input
R/±(R–Y)IN	4	R or (R–Y) signal input
G/Y IN	5	G or Y signal input
B/±(B–Y)IN	6	B or (B–Y) signal input
VINT	7	internal voltage supply
SYNC1	8	synchronization input for Channel 1
ON	9	ON input
R/–(R–Y)IN	10	R or –(R–Y) signal input
G/Y IN	11	G or Y signal input
B/–(B–Y)IN	12	B or –(B–Y) signal input
SDA	13	serial data input/output; I²C-bus
SCL	14	serial clock input; I²C-bus
S0	15	address selection input 0
S1	16	address selection input 1
S2	17	address selection input 2
V_P	18	supply voltage
B/–(B–Y)OUT	19	B or –(B–Y) signal output
G/Y OUT	20	G or Y signal output
R/–(R–Y)OUT	21	R or –(R–Y) signal output
GND	22	ground
SYNC	23	synchronization output
CLAMP	24	clamping pulse generator input/output

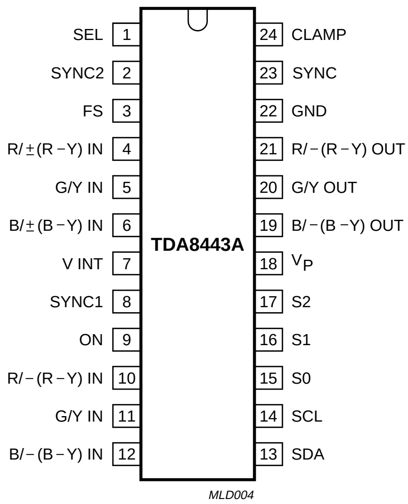


Fig.2 Pin configuration.

BLOCK DIAGRAM

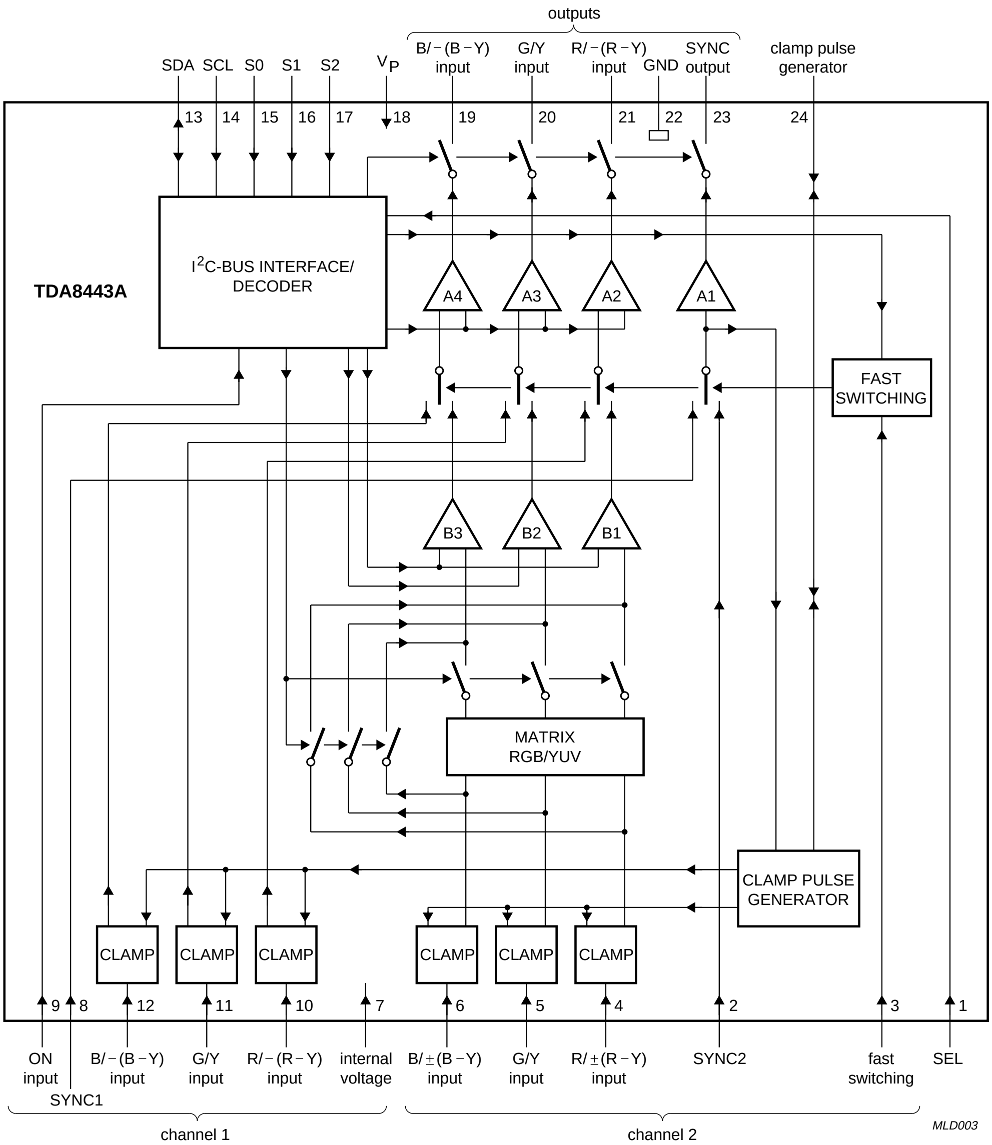


Fig.1 Block diagram.

FEATURES

- Two RGB/YUV selectable clamped inputs with associated synchronization
- RGB/YUV matrix
- 3-state switching with an OFF-state
- Selectable gain
- I^2C-bus or non-I^2C-bus mode
- Address selection for 7 devices
- Fast switching.

GENERAL DESCRIPTION

The TDA8443A is a general purpose two-channel switch for YUV or RGB signals. One channel provides matrixing from RGB to YUV, which can be bypassed.

The IC is controlled via I^2C-bus by seven different addresses or can be used in a non-I^2C-bus mode. In the non-I^2C-bus mode, control of the circuit is achieved by DC voltages.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage (pin 18)		10.8	12.0	13.2	V
I_P	supply current		–	65	90	mA
RGB/YUV channels						
$Z_{19\text{-}22}$	output impedance (pin 19)		–	7	30	Ω
$Z_{20\text{-}22}$	output impedance (pin 20)		–	7	30	Ω
$Z_{21\text{-}22}$	output impedance (pin 21)		–	7	30	Ω
B	bandwidth	–3 dB; mode 0 or 2	–	25	–	MHz
		+3 dB; mode 0 or 2	–	12	–	MHz
		±3 dB; mode 1	–	10	–	MHz
$V_{O(p-p)}$	maximum output amplitude of YUV signals (peak-to-peak value)	gain × 1	2.1	–	–	V
		gain × 2	4.2	–	–	V
T_{amb}	operating ambient temperature		0	–	+70	°C

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA8443A	DIP24	plastic dual in-line package; 24 leads (600 mil)	SOT101-1